formed at least on a side of said second gate insulation film and having said second relative permittivity, wherein

when a cross-section on a side of said first channel is S1, a cross-section on a side of said first gate electrode is S2, a cross-section on a side of said second channel is S3, and a cross-section on a side of said second gate insulation film is S4, a condition of:

$$S2/S1 > S4/S3$$

is satisfied.

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-12 are pending in the present application with Claims 1, 9 and 10 having been amended by the present amendment.

In the outstanding Office Action, Claims 1 and 9 were rejected under 35 U.S.C. § 102(b) as anticipated by Katoh; Claims 2, 4-8 and 11 were rejected under 35 U.S.C. §103(a) as unpatentable over Krivokapic et al in view of Katoh; Claims 3 and 10 were rejected under 35 U.S.C. §103(a) as unpatentable over Katoh; and Claim 12 was indicated as allowable if rewritten in independent form.

Applicants thank the Examiner for the indication of allowable subject matter.

Claims 1 and 9 stand rejected under 35 U.S.C. §102(b) as anticipated by Katoh. This rejection is respectfully traversed.

Amended Claim 1 is directed to a semiconductor device including a channel of a first conductivity type formed on a surface layer of a semiconductor substrate, a source and a drain of a second conductivity type formed on both sides of the channel, a gate insulation

film with a first relative permittivity formed at least on the channel directly or through a buffer isolation film, a gate electrode formed on the gate insulation film, and a side insulation film formed at least on a side of the gate insulation film and having a second relative permittivity which is smaller than the first relative permittivity. Further, when a first length, which is a length of the gate insulation film adjacent to the surface layer on the gate electrode side along a channel length direction is L1, a second length which is a length of the gate insulation film adjacent to the surface layer on the channel side along the channel length direction is L2, and a third length, which is a length of a bottom part of the gate electrode is L3, the length L1 is longer than a length L2, and a length L3 is longer than the length L1. Claim 9 includes a similar feature but recites that a length of a bottom part of the gate electrode along a channel length direction is longer than a length of an upper part of the gate insulation film along a channel length direction.

This feature is shown in a non-limiting example of Figure 22H, in which the length of the gate insulation film 14 adjacent to the surface layer on the gate electrode 15 side along the channel length direction is longer than the length of the gate insulation film 14 adjacent to the surface layer on the channel side along the channel direction, and the length of the bottom part of the gate electrode 15 is longer than the length of the gate insulation film 14 adjacent to the surface layer on the gate electrode 15 side along the channel length direction.

The outstanding Office Action indicates Katoh discloses a semiconductor device including a channel 126, a source 105, a drain 106 and a gate insulation film 128 and cites Figures 1 and 2. However, Applicants note Figure 2 of Katoh is a partial cross-sectional view along the lines II-II in Figure 1 (i.e., along a direction normal to a channel length direction). Claims 1 and 9 of the present invention recite a relationship among lengths of, for example, the first to third (or second) parts (area) along a channel length direction. However,

as is apparent from Figure 1 of Katoh, the lengths thereof are the same. This differs from the claimed invention which recites that the length L1 is longer than the length L2, and the length L3 is longer than the length L1.

Accordingly, it is respectfully submitted independent Claims 1 and 9 and each of the claims depending therefrom patentably define over Katoh.

Claims 2, 4-8 and 11 stand rejected under 35 U.S.C. §103(a) as unpatentable over Krivokapic et al in view of Katoh. This rejection is respectfully traversed.

Claims 2 and 4-8 depend on Claim 1, and Claim 11 depends on Claim 10 (which has also been amended to include subject matter similar to that recited in Claim 9 as discussed below). Further, it is respectfully submitted Krivokapic et al also do not teach or suggest the claimed lengths. Accordingly, it is respectfully requested this rejection also be withdrawn.

Claims 3 and 10 stand rejected under 35 U.S.C. §103(a) as unpatentable over Katoh. This rejection is respectfully traversed.

Claim 3 depends on Claim 1, which as discussed above is believed to be allowable. Further, Claim 10 is directed to a semiconductor device including a plurality of first and second MOS transistors. Katoh do not teach or suggest a plurality of first and second MOS transistors. Accordingly, it is respectfully submitted independent Claim 10 and each of the claims depending therefrom are also allowable.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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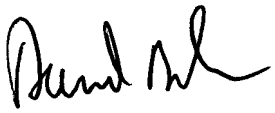

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IN THE CLAIMS

--1. (Three Times Amended) A semiconductor device comprising:

a channel of a first conductivity type formed on a surface layer of a semiconductor substrate;

a source and a drain of a second conductivity type formed on both sides of the channel;

a gate insulation film with a first relative permittivity formed at least on said channel directly or through a buffer insulation film;

a gate electrode formed on said gate insulation film; and

a side insulation film formed at least on a side of said gate insulation film and having a second relative permittivity which is smaller than the first relative permittivity, wherein

[when a first area of said gate insulation film adjacent to said gate electrode is S1, a second area of said gate insulating film adjacent to said channel is S2, and a third area of a bottom part of said gate electrode is S3,

the area S1 is larger than the area S2, the area S3 is larger than the area S1, a part of the third area S3 is connected to said gate insulating film, and the other part of the third area S3 is not connected to said gate insulating film] when a first length, which is a length of the gate insulation film adjacent to said surface layer on the gate electrode side along a channel length direction, is L1, a second length, which is length of the gate insulation film adjacent to

said surface layer on said channel side along the channel length direction, is L2, and a third length, which is a length of a bottom part of said gate electrode, is L3,

the length L1 is longer than the length L2, and the length L3 is longer than the length L1.

9. (Three Times Amended) A semiconductor device comprising:

a channel of a first conductivity type formed on a surface layer of a semiconductor substrate;

a source and a drain of a second conductivity type formed on both sides of the channel;

a gate insulation film with a first relative permittivity formed at least on said channel directly or through a buffer insulation film;

a gate electrode formed on said gate insulation film; and

a side insulation film formed at least on a side of said gate insulation film and having a second relative permittivity which is smaller than the first relative permittivity,

wherein

an electric flux density in said gate insulation film on a side towards the channel side is more dense than an electric flux density in said gate insulation film on a side towards the gate electrode, [and]

an area of a bottom part of said gate electrode is larger than an area of an upper part of said gate insulation film, and

a length of a bottom part of said gate electrode along a channel length direction is longer than a length of an upper part of said gate insulation film along a channel length direction.

10. (Three Times Amended) A semiconductor device comprising:

a plurality of first MOS transistors, each of said first MOS transistors including[,

]a first channel of a first conductivity type formed on a surface layer of a semiconductor substrate, [

]a first source and a first drain of a second conductivity type formed to both sides of said first channel, [

]a first gate insulation film with a first relative permittivity formed at least on the first channel directly or through a buffer insulation film, [

]a first gate electrode formed on said first gate insulation film, and [

]a first side insulation film formed at least on a side of said first gate insulation film and having a second relative permittivity which is smaller than the first relative permittivity; and

a plurality of second MOS transistors, each of said second MOS transistors including[,

] a second channel of the first conductivity type formed on a surface layer of said substrate, [

]a second source and a second drain of the second conductivity type formed on both sides of said second channel, [

]a second gate insulation film with the first relative permittivity formed at least on said second channel directly or through a buffer insulation film, [

]a second gate electrode formed on said second gate insulation film, and [

]a second side insulation film formed at least on a side of said second gate insulation film and having said second relative permittivity, wherein

[wherein,]when a cross-section on a side of said first channel is S1, a cross-section on a side of said first gate electrode is S2, a cross-section on a side of said second channel is S3, and a cross-section on a side of said second gate insulation film is S4, a condition of:

$$S2/S1 > S4/S3$$

is satisfied[, and

an area of a bottom part of said first gate electrode is larger than an area of an upper part of said first gate insulation film and an area of a bottom part of said second gate electrode is larger than an area of an upper part of said second gate insulation film].--